WHAT IS CLAIMED IS:

1. A method for determining existence of a loss-of-signal (LOS) condition for an input data stream, the method comprising:

comparing signal strength of a plurality of data bits of the input data stream to a signal strength threshold level and generating an indication thereof;

determining a count value according to the indication; and

generating a loss-of-signal indication according to the count value.

2. The method as recited in claim 1 further comprising sampling the input data stream to obtain the plurality of data bits, the sampling rate being below a data rate of the input data stream.

3. The method as recited in claim 1 further comprising sampling the input data stream to obtain the plurality of data bits at a sampling rate equal to or higher than a data rate of the input data stream.

4. The method as recited in claim 1 wherein asserting the loss-of-signal indication comprises comparing the count value to a threshold count level.

5. The method as recited in claim 4 wherein the threshold count level is programmable.

6. The method as recited in claim 4 wherein the threshold count varies according to an indication of the signal strength threshold level.

7. The method as recited in claim 4 wherein the threshold count varies to provide hysteresis in generating the loss-of-signal indication.

8. The method as recited in claim 7 wherein the threshold count increases when the loss-of-signal indication is asserted.

9. The method as recited in claim 1 wherein the comparing further comprises:

latching a first value in a register when the signal strength of a data bit of the input data stream is above the signal strength threshold level and latching a second value in the register when the signal strength of the data bit is below the signal strength threshold level.

10. The method as recited in claim 9 further comprising:

supplying the data bit to an amplifier, which is coupled to supply the data bit to the register; and

supplying an offset to the amplifier, the offset being at a level to cause the register to store the first value when the signal strength of the data bit is above the signal strength threshold level and to store the second value when the signal strength of the data bit is below the signal strength threshold level.

11. The method as recited in claim 10 further

supplying a digital value indicative of the offset to at least one digital to analog converter (DAC); and

supplying as the offset an output from the at least one DAC.

12. The method as recited in claim 10 wherein first portion of the digital signal is supplied to a first DAC and a second portion to a second DAC, the offset being formed from outputs of the first and second DACs.

13. The method as recited in claim 12 wherein at least a portion of the digital signal supplied to the first and second DACs overlap.

14. The method as recited in claim 9 wherein the register is clocked at a rate below a data rate of the input data stream.

15. The method as recited in claim 14 further comprising decimating an output of the register and supplying the decimated output as a count control signal to a counter to determine the count value.

16. The method as recited in claim 15 wherein the count value is the number of data bits having a signal strength above the signal strength threshold level.

17. The method as recited in claim 15 wherein the decimating comprises:
supplying an output of the register to a one-to-transition converter;
dividing an output of the one-to-transition converter;
supplying the divided output to a transition-to-one converter; and
supplying an output of the transition-to-one converter as the count control signal.

18. The method as recited in claim 1 wherein the comparing is for a predetermined number of data bits.

19. The method as recited in claim 1 wherein the comparing is performed for each of four phases of a clock before a decision is made that a loss of signal condition exists.

20. The method as recited in claim 1 wherein the comparing is performed for at least one phase of a clock before a decision is made that a loss of signal condition exists.

21. The method as recited in claim 1 wherein the comparing is repeated for a signal strength threshold for both ones and zeros before a decision is made that a loss of signal condition exists.

22. The method as recited in claim 21 wherein the determining for both ones and zeros is repeated for each of for four phases of a clock before a decision is made that a loss of signal condition exists.

23. The method as recited in claim 1 wherein the signal strength threshold level is programmable via a communication port on the integrated circuit.

24. The method as recited in claim 1 further comprising calibrating the signal strength threshold level each time prior to determining whether the signal strength of a predetermined number of data bits is above or below the signal strength threshold level.

25. The method further comprising 24 further comprising calibrating the signal strength threshold for ones before testing for ones and calibrating the signal strength threshold for zeros before testing for zeros.

26. The method further comprising 24 wherein the signal strength threshold for zeros is generated by negating the signal strength threshold generated for ones.

27. The method as recited in claim 1 wherein the signal strength threshold level is defined by an analog signal on an input terminal.

28. A method for determining existence of a loss-of-signal condition, the method comprising:

determining for a plurality of data bits of the input data stream whether a signal strength of each of the data bits is above or below a signal threshold level; and

determining that a loss of signal condition exists if a predetermined number of the data bits have signal strength below a count threshold level.

29. A method for determining existence of a loss-of-signal (LOS) condition comprising:

sampling input data;

comparing a magnitude of the sampled input data to a threshold signal strength level; and

asserting a LOS indication if a number of samples, over a predetermined time period, having a signal strength less than the threshold signal strength level, is more than a predetermined value.

30. An integrated circuit for receiving input data and generating a loss-of-signal (LOS) indication associated therewith, comprising:

a sample circuit coupled to sample the input data and store a first value when signal strength magnitude of the sampled input data is above a signal strength threshold level and store a second value when signal strength magnitude of the input data is below the signal strength threshold level; and

a counter circuit coupled to count according to an output of the sample circuit.

31. The integrated circuit as recited in claim 30 further comprising a comparison circuit coupled to compare an output of the counter circuit and a threshold count value and generate the loss-of-signal indication according to the comparison.

32. The integrated circuit as recited in claim 31 wherein the threshold count value varies according to an indication of the signal strength threshold level.

33. The integrated circuit as recited in claim 31 wherein the threshold count varies to provide hysteresis in generating the loss-of-signal indication.

34. The integrated circuit as recited in claim 33 wherein the threshold count increases when the loss-of-signal indication is asserted.

35. The integrated circuit as recited in claim 30 wherein the sample circuit includes an amplifier, the amplifier being coupled to receive an offset, the offset being at a level to cause the sample circuit to store the first value when the signal strength magnitude of the input signal is above the signal strength threshold level and to store the second value when the signal strength magnitude of the input signal is below the signal strength threshold level.

36. The integrated circuit as recited in claim 35 further comprising a digital control block coupled to supply a digital value of the offset signal; and and at least one digital to analog converter coupled to the digital value of the offset signal and to the amplifier.

37. The integrated circuit as recited in 30 further comprising: a decimator circuit coupled to the sample circuit, an output of the decimator circuit coupled as a count control signal for the counter circuit.

38. The integrated circuit as recited in claim 37 wherein the decimator circuit comprises:
a one-to-transition converter circuit;
a divide by n circuit coupled to the one-to-transition converter circuit;
a transition-to-one converter coupled to receive an output of the divide by n circuit and coupled to supply an output of the transition to one converter as the count control signal.

39. The integrated circuit as recited in claim 37 further comprising a multiple clock phase generator circuit coupled to supply to the register circuit and the decimator circuit one of a plurality of phases of a clock.

40. The integrated circuit as recited in claim 30 wherein the signal strength threshold level is programmable.

41. The integrated circuit as recited in claim 30 wherein the signal strength threshold level is programmable via a serial communications port on the integrated circuit.

42. An apparatus detecting a loss-of-signal (LOS) condition comprising:
means for determining for a plurality of data bits of an input data stream whether a signal strength magnitude of each of the data bits is above or below a signal threshold level; and

means for determining that a loss of signal condition exists if a predetermined number of the data bits have signal strength below a threshold level.

43. An apparatus detecting a loss-of-signal (LOS) condition comprising:

means for sampling an input data stream;

means for comparing signal strength magnitude of the sampled input data stream to a threshold signal strength level; and

means for asserting a LOS indication if a number of samples having signal strength less than the threshold signal strength level is less than a predetermined value.